

REMARKS

This Response is intended as a complete response to the Office Action dated December 28, 2006. In view of the following discussion, the Applicants submit that all claims are presently in condition for allowance.

CLAIM REJECTIONS

35 USC §103

A. Claims 1-18 and 36-53

Claims 1-18 and 36-53 stand rejected under 35 USC §103 as being unpatentable over US Patent No. 6,625,497, issued September 23, 2003, to *Fairbairn, et al.* (hereinafter *Fairbairn*) in view of US Patent Application Publication No. 2004/0078108, published April 22, 2004, to *Choo, et al.* (hereinafter *Choo*) and further in view of US Patent 6,567,717, issued May 20, 2003, to *Krivokapic, et al.* (hereinafter *Krivokapic*) and US Patent Application No. 2004/0087041 published May 6, 2004 to *Perry, et al.* (hereinafter *Perry*). The Applicants respectfully disagree.

Independent claims 1 and 36 recite limitations not taught or suggested by any combination of the cited art. *Fairbairn* teaches a semiconductor processing module with integrated feedback/feed forward metrology. Specifically, *Fairbairn* teaches reducing critical dimension (CD) variation by feeding back information gathered during inspection of a wafer (e.g., after photoresist development) to upcoming lots that will be going through the photolithography process, and by feeding forward information to adjust the next process the inspected wafer will undergo (e.g., the etch process). (*Fairbairn*, col. 4, ll. 40-46.) *Fairbairn* further teaches taking post-etch CD measurements and optionally reviewing the wafer if a significant variation from normal post-etch data is observed. (*Id.*, col. 12, ll. 24-34; col. 13, ll. 55-65.)

Choo teaches scatterometry techniques for measuring one or more dimensions of a first integrated circuit during a fabrication process. The measurements may be used feed forward or feed back information that may be utilized to adjust operating parameters of other processing components to which the same or other die will be subjected. (See *Choo*, p. 5, ¶ [0042].)

However, *Choo* fails to teach or suggest a modification of the teachings of *Fairbairn* that would yield a process including executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1, or executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass, as recited in claim 36.

Krivokapic is cited for the proposition that it teaches that, after a post-etch measurement, wafers may be returned for further etching if under-etched. However, *Krivokapic* merely teaches and suggests further etching of an under-etched workpiece if, and only if, the desired etch results were not obtained during a first etch, and fails to teach a multi-pass process as recited in the claims. The Examiner quotes *Krivokapic* as stating “non-conforming post-etch wafers may be returned for further etching if underetched” and further asserts that this statement “in effect describes a multi-pass process when the under-etch is performed by design.” (Office Action, p. 6, ll. 11-15.) The Applicants respectfully disagree.

The Examiner appears to be using hindsight reconstruction to assert alleged teachings of *Krivokapic*. Specifically, the complete quote from *Krivokapic* is that “[n]onconforming, post-etch wafers may be thrown away if over-etched, or returned for further etching (re-work) if under-etched.” Accordingly, it is clear that *Krivokapic* merely recites that, after measurement, if the wafer is over-etched and unsalvageable, then the wafer may be thrown away, but if the wafer is under-etched and may be saved, then it may be returned for re-work. Such re-work is not a multi-pass process as defined in the present claims. *Krivokapic* is silent with respect to performing a multi-pass process as defined in the claims. As such, *Krivokapic* clearly fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1, or executing a multi-pass process, wherein the substrate is processed more than once by at least one

measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass; and measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process, as recited in claim 36.

Perry is cited to show a control etch method based on an *in-situ* thickness measurement step. However, *Perry* fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1, or executing a multi-pass process, wherein the substrate is processed more than once by at least one measurement process, an etch process and at least one pre-etch process and/or at least one post-etch process while forming at least one structure on the substrate, where each time the substrate is processed by the etch process is a pass; and measuring at least one pre-etch dimension and at least one post-etch dimension of at least one structure on the substrate, during each at least one measurement process, as recited in claim 36. Hence, *Perry* fails to teach or suggest a modification of *Fairbairn*, *Choo*, and *Krivokapic* of that would yield the limitations recited in claims 1 and 36. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that independents claim 1 and 36, and claims 2-18 and 37-52, respectively depending therefrom, are patentable over *Fairbairn* in view of *Choo*, and further in view of *Krivokapic* and *Perry*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

B. Claims 19-21

Claims 19-21 stand rejected under 35 U.S.C. §103 as being unpatentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry*, as applied above to claim 1, and further in view of US Patent Application No. 2003/0022510 published January 30, 2003 to *Morgenstern* (hereinafter *Morgenstern*). The Applicants respectfully disagree.

Independent claim 1, from which claims 19-21 depend, recites limitations not taught or suggested by any permissible combination of the cited art. The patentability of claim 1 over the combination of *Fairbairn*, *Choo*, *Krivokapic*, and *Perry* is discussed above. The Examiner cites *Morgenstern* to show a process of forming a capacitive trench structure with a polysilicon electrode layer wherein the etch process is performed with an HBr and Cl₂ chemistry.

However, *Morgenstern* fails to teach or suggest executing a multi-pass process wherein the substrate is processed more than once by a measurement process, an etch process, and at least one post-etch process while forming the at least one structure, as recited in claim 1. Hence, *Morgenstern* fails to teach or suggest a modification of *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* that would yield the limitations recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established as the combination of the cited references fails to yield the limitations recited in the claims.

Thus, the Applicants submit that claims 19-21 are patentable over *Fairbairn* in view of *Choo*, *Krivokapic*, and *Perry* and further in view of *Morgenstern*. Accordingly, the Applicants respectfully request that the rejection be withdrawn and the claims allowed.

CONCLUSION

Thus, the Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If the Examiner believes that there are any unresolved issues, it is requested that the Examiner telephone Mr. Alan Taboada at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

March 28, 2007
Date

/ Alan Taboada /
Alan Taboada, Attorney
Reg. No. 51,359
(732) 935-7100
Moser IP Law Group
1040 Broad St.
Shrewsbury, NJ 07702